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Patentanmeldung Nr. Patent application No. Demande de brevet n°

99480131.4

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

I.L.C. HATTEN-HECKMAN

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LA HAYE, LE

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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

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Built-in self test system and method for high speed clock and data recovery circuit

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BUILT-IN SELF TEST SYSTEM AND METHOD FOR HIGH SPEED CLOCK AND DATA RECOVERY CIRCUIT

Technical field

The present invention relates to systems for testing clock and data recovery circuits, and more particularly to a built-in self test system.

Background art

In digital systems, digital data is typically handled with an associated clock signal. The clock provides timing necessary to allow digital circuitry to operate on digital data. When data are transmitted over a communications link, it is generally inefficient to also transmit the associated clock signal. This inefficiency has led to communications systems which transmit the data alone without the clock. Therefore, it is typical for fiber optic communication links to require that the clock signal at the receiving end of the link be extracted from the incoming data signal. To obtain the necessary clock

at the receiving end, these systems employ clock and data recovery circuits. The clock and data recovery circuit derives the clock signal from the received digital data. Conventional clock and data recovery circuits are often implemented using phase-locked loops. In phase-locked loops, a reference clock is generated at the frequency of the received data using a voltage controlled oscillator (VCO). The phase-locked loop is often integrated onto a single chip along with logic circuits providing other link adapter functions.

In addition to clock recovery circuits, communications links often utilize serializers and deserializers circuits. Serializers on the transmitting side serialize the parallel data in a bit stream. Deserializers at the receiving end parallelize the serial data stream transmitted over the communications link. These parallel data are typically defined by bytes or words that make up the serial stream.

To eliminate defects from integrated circuits including logic circuits a well-known method consists to place observation latches (the famous LSSD latches) which are connected together to allow to scan out each signal which is generated internally. Test patterns sequences are performed at wafer level and if responding patterns do not match the test patterns, the failed circuits are sorted. Unfortunately this method cannot be used to detect defects in the analog circuits.

Conventional methods to test analog components consist in verifying the functionality of the analog circuitry by way of an external test equipment. Such method need that the chip be previously encapsulated before being tested at board level.

The general state of the prior art with respect to solving the aforementioned testing problem may be best illustrated and understood with reference to the several patents to be described immediately hereinafter.

In U.S. Patent No 5,295,079 from Wong a digital testing system for very high frequency PLLs is proposed. The testing system allows the test of a PLL connected to an external digital tester via a bi-directional bus. The digital tester is an intelligent digital hardware that configures the PLL and extracts and interprets data from the PLL.

In U.S. Patent No 5,729,151 from Zoerner, the test of a phase lock loop within an integrated circuit is performed by an external testing device having access to an address/data bus coupled to both the PLL and a timer module which is utilized as a frequency counter for counting the number of clock pulses outputted from the PLL.

The aforementioned conventional methods employ an external testing equipment to test the PLL. Whereas such solutions are efficient to test high frequency PLLs, they are heavy in terms of cost and people, and in addition the permanent performance evolution of the products requires that the test equipment be adapted.

Alternative methods consist in using Built-in Self-Test (BIST) circuits.

In U.S. Patent No 5,802,073 from Platt, a built-in self-test (BIST) system for testing a network interface integrated circuit is disclosed. The BIST includes a random number generator to generate test data, and to monitor data going from a receiver of the network interface back to the BIST. The data is compressed into one number and compared with a predetermined signature in a signature analyzer. The BIST uses a functional system block for in-system diagnostic at system speed at a functional level as opposed to gate level.

In U.S. Patent No 5,835,501 from Dalmia, a built-in self-test circuit is provided to perform jitter tolerance tests on a clock and data recovery unit by using a pseudo-random data

generating apparatus. The test is comprised of the steps of generating a jitter clock, using the jitter clock to generate a test data stream, feeding the test data stream to the clock and data recovery unit and determining the number of bits errors in the recovered data stream. This methods requires that all the recovered bits be examined to determine the famous Bit Error Rate (BER) which is thus a time consuming solution.

Accordingly, it would be desirable to be able to provide a functional wafer level test system and method which allows full fault coverage of a clock and data recovery circuit.

Summary of the invention

The present invention provides a built-in self test apparatus for testing a clock and data recovery circuit which operates with high speed phase lock loop. The built-in circuit comprises data generating means for generating a test data byte and serializing means coupled to the data generating means for converting the test data byte into serial test data. The clock and data recovery means are coupled to the output of the serializing means for recovering the clock and test data from the serial test data. A deserializing means coupled to the output of the clock and data recovery means converts the recovered serial test data into a recovered test data byte, and analyzing means connected to the output of the deserializing means compares the recovered test data byte to the initial test data byte.

In a commercial application, the invention is preferably used in a high speed telecommunication framer which fulfill the requirements of the SONET technology.

It is another object of this invention to provide a method for testing a clock and data recovery circuit comprising the steps of:

- generating an initial test data byte,
- inputting the test data byte to a serializer for conversion into serial test data,
- sending the serial test data to the clock and data recovery circuit for recovering the clock and the test data,
- inputting the recovered test data to a deserializer for conversion into a recovered test data byte, and
- comparing the recovered test data byte to the initial test data byte.

Brief description of the drawings

Fig.1-a shows a general block diagram of a preferred data communication system into which is incorporated the BIST circuit of the invention.

Fig.1-b illustrates a SONET frame structure.

Fig.2 shows a schematic block diagram of the built-in self test circuit of the present invention.

Fig.3 is a flow chart illustrating the state machine process to operate the circuit of figure 2.

Detailed description of the invention

Referring to the drawings, and more particularly to Fig.1, a general block diagram of part of a preferred data communication system into which is incorporated the BIST circuit of the invention is now described. The diagram is simplified for the purpose of understanding the principles of the invention. The system 100 is part of an optical

transmission device and comprises a framer unit 110, a serializer/deserializer unit 120, an optical transceiver unit 130 and an optical fiber 140. Preferably such system is used in optical networking with SONET/SDH technology.

Synchronous Optical Network (SONET) is a U.S. standard for the international operations of optical networks. Fiber optics connect Asynchronous Transfer Mode (ATM), frame relay, Ethernet and other high-speed networks. SONET is a primary network transport mechanism of ATM systems. The SONET core can mix packages, or frames from different sources and carry them over a network. The basic structure in SONET is a frame of 810 bytes which is sent every 125 microseconds. This allows a single byte within a frame to be part of a 64 kilobits per second (Kbps) digital voice channel. Since the minimum frame size is 810 bytes then the minimum speed at which SONET operates is 51.84 megabits per second (mbps). The SONET signaling hierarchy is stated as Optical Carrier (OC) levels with OC-1 as the foundation transmission rate (51.840 Mbps).SONET is capable of reaching transmission rates of gigabits per second by using multiples of this rate (OC-3 level at 155.520 Mbps, OC-12 level at 622.080 Mbps, and OC-48 level at 2488.32 Mbps are currently the most widely supported multiples of OC-1).

The basic frame is called the Synchronous Transport Signal Level (STS-1). It is conceptualized in a two-dimensional frame as containing 9 rows of 90 columns each as shown in Figure 1-b, but in reality it is a string of bits. The frame is transmitted row by row, from the top left to the bottom right. The first three columns of every row are used for administration and control of the system. Multiple STS-1 frames can be byte-multiplexed together to form higher-speed signals. When this is done they are called STS-2, STS-3 where the numeral suffix indicates the number of STS-1 frames that are present.

Referring again to figure 1, in normal mode of data transmission, a transmit serial bit stream in electrical form is presented to the optical transceiver 130 which encodes the data appropriately for transmission over the optical fiber 140. The transmit serial bit stream is issued from the serializer 120 which converts parallel frames to be transmitted into serial bit stream.

When operating on receiving path, the optical signal is fed to the optical transceiver for conversion in electrical form into a receive serial bit stream. The receive serial bit stream is recovered within a clock and data recovery circuit contained within the SER/DES unit 120. The recovered serial data are converted into receive parallel data by the deserializer 120. The receive parallel data are latter processed within framer 140.

In test mode, the SER/DES unit 120 operates internally as will be described in more detail with reference to figure 2. Generally, test parallel data are internally generated by a pattern generator in lieu of the operational data. Next they are fed to the serializer, and the serial data are wrapped to the clock and data recovery circuit for extracting the clock and retiming the data. The recovered data are next input to the deserializer, and the rebuilt bytes obtained by the deserialization process are compared to the initial test data generated by the pattern generator. The patterns are predefined to be made of a frame header signature followed by sequence of bits containing a maximum number of transitions such as '01010101...'. The clock and data recovery unit may thus be easily lock on the data stream. In the case of a SONET frame, the frame header signature can be made of 6 bytes generally denoted 'A1,A1,A1,A2,A2,A2'. The test of the clock and data recovery circuit is performed by detecting this frame header in the deserializer circuit.

However, the test patterns may be adapted to fulfill the requirements of other technology.

Referring now to Fig.2 a schematic block diagram of a preferred embodiment of the built-in self test circuit 200 of the present invention is described. The circuit 200 comprises a serializer 202 to input operational parallel data issued from internal circuitry or parallel test data generated by a pattern generator 204. A first multiplexer 206 is provided and has the operational parallel data and the test patterns as data inputs and has an internal selection bit value (B-ENB 208) as a data select input. A second multiplexer 210 having serial data received from optical transmission link and the output of the serializer 202 as data inputs is also provided. The second multiplexer also inputs the internal selection bit value (B-ENB 208) as data select input. The test patterns and the output of the serializer 202 are the selected data inputs for respectively the first and the second multiplexer (206,210) when the internal selection bit signal is set to activate the self test mode. A clock and data recovery circuit 212 is connected to the output of the second multiplexer 210 to perform the clock extraction and data regeneration in a well-known manner. A deserialiser 214 connected to the output of the clock and data recovery circuit parallelizes the recovered serial data. A state machine 216 connected to the output of the deserializer comprises means to compare the recovered data bytes to the initial test pattern. A signature signal (SIG) is generated to validate the reconstruction of the initial data pattern and to stop the test data generation by disabling the pattern generator. The state machine 216 further includes conventional time out counters. A first counter is initialized before the test is performed to wait for the phase lock loop to lock to a predetermined frequency. A second counter allows during a predefined period of time that numerous test patterns be repetitively generated as long as the recovered test patterns do not match the expected ones. Preferably, the pattern generator is a programmable circuit to provide different test sequences.

Figure 3 is a flow chart for illustrating the state machine process of the invention.

Though not shown on the initial state (300), the built-in self test sequence is started by the assertion of the internal selection bit (B-ENB) to place the circuit 200 in test mode. A first test frame is provided to the clock and data recovery circuit via the serializer as previously described.

Thereafter the state machine enters a lock state (302) to wait for the voltage control oscillator contained in the CDR circuit to lock to the reference frequency. A first count state (304) illustrates running of a first time counter to loop back (branch No) to lock state (302) until the VCO is lock. If the counting ends before the VCO is lock (branch Yes) the process aborts (state 314).

Back to lock state (302), when the VCO is lock to the reference frequency, a first test frame which has been serialized thru serializer (202) is recovered within the CDR (212) and a first result test frame is analyzed on check state (308). The test loops to state (306) to generate continuously the test pattern until the serial data stream is on phase with the VCO. If the result test frame matches the initial test frame (the expected signature), the test process is ended (state 310).

Thus test patterns are sequentially generated until the result of the comparison is 'match' (state 310) or until the time counter is ended (state 312). If the time counter is ended before a successful comparison test the process aborts (state 314).

It is to be noted that no specific test pattern have been mentioned for operating the built-in self test of the invention. It is an advantage of the invention that different types of test pattern may be applied to check the functionality of the PLL as well as its stability in case of programmed patterns with low transition rate.

In one embodiment, the BIST circuit is in the form of a high level logic description (VHDL) code to describe the function of the logic circuitry as described above. However, logic circuits may be designed at the gate level in other embodiments.

While the invention has been particularly shown and described with reference to a preferred embodiment thereof, it will be understood by those skilled in the art that various change in form and details may be made without departing from the spirit and scope of the invention.

Claims

1. A built-in self test circuit (200) for testing a clock and data recovery circuit (212) comprising:

   - data generating means (204) for generating a test data byte,
   - serializing means (202) coupled to the data generating means for converting the test data byte into serial test data,
   - clock and data recovery means (212) coupled to the output of the serializing means for recovering the clock and test data from the serial test data,
   - deserializing means (214) coupled to the output of the clock and data recovery means for converting the recovered serial test data into a recovered test data byte, and
   - analyzing means (216) connected to the output of the deserializing means for comparing the recovered test data byte to the test data byte.

2. The circuit of claim 1 wherein said clock and data recovery circuit comprises a phase lock loop.

3. The circuit of claim 1 or 2 further comprising a first multiplexer (206) coupled to the serializing means for inputting operational data byte or said test data byte upon setting of a data selection signal (B-ENB 208).

4. The circuit of claim 1,2 or 3 further comprising a second multiplexer (210) coupled to the clock and data recovery circuit for inputting operational serial data or said serial test data upon setting of a data selection signal (B-ENB 208).

5. The circuit of anyone of claims 1 to 4 wherein said test data byte is in the form of a SONET frame, and said analyzing means comprises means for detecting the start of a SONET frame.

6. The circuit of anyone of claims 1 to 5 further comprising a state machine to control said generating means and said analyzing means.

7. The circuit of anyone of claims 1 to 6 wherein said data generating means is a programmable data generator.

8. A method for testing a clock and data recovery circuit (212) comprising the steps of:

- generating an initial test data byte,
- inputting the test data byte to a serializer for conversion into serial test data,
- sending the serial test data to the clock and data recovery circuit for recovering the clock and test data from the serial test data,
- inputting the recovered serial test data to a deserializer for conversion into a recovered test data byte, and
- comparing the recovered test data byte to the initial test data byte.

9. The method of claim 8 wherein said clock and data recovery circuit comprises a phase lock loop.

10. The method of claim 8 or 9 further comprising an initial step of waiting for a predetermined period of time to allow said phase lock loop to lock to a predetermined frequency before beginning of said generating step.

11. The method of anyone of claims 8 to 10 further comprising:
    - generating a new test data byte, and
    - repeating said serializing, recovering, deserializing and analyzing steps until the recovered test data byte matches the test data byte.

12. The method of claim 11 wherein said step of generating a new test data byte and said repeating step are performed until a counter reaches a predetermined number of pulses.

13. The method of anyone of claims 8 to 12 wherein said generating step and said analyzing step are controlled by a state machine.

14. The method of claim 13 wherein said counter is included within said state machine.

Abstract

BUILT-IN SELF TEST SYSTEM FOR HIGH SPEED CLOCK AND DATA RECOVERY CIRCUIT

A built-in self test system for testing a clock and data recovery circuit is disclosed. The present invention provides a built-in self test circuit which operates with high speed phase lock loop. The built-in circuit comprises data generating means for generating a test data byte and serializing means coupled to the data generating means for converting the test data byte into serial test data. The clock and data recovery means are coupled to the output of the serializing means for recovering the clock and test data from the serial test data. A deserializing means coupled to the output of the clock and data recovery means converts the recovered serial test data into a recovered test data byte, and analyzing means connected to the output of the deserializing means compares the recovered test data byte to the initial test data byte.

Fig. 2

FR 9 99 060
Bonneau et al
1/4

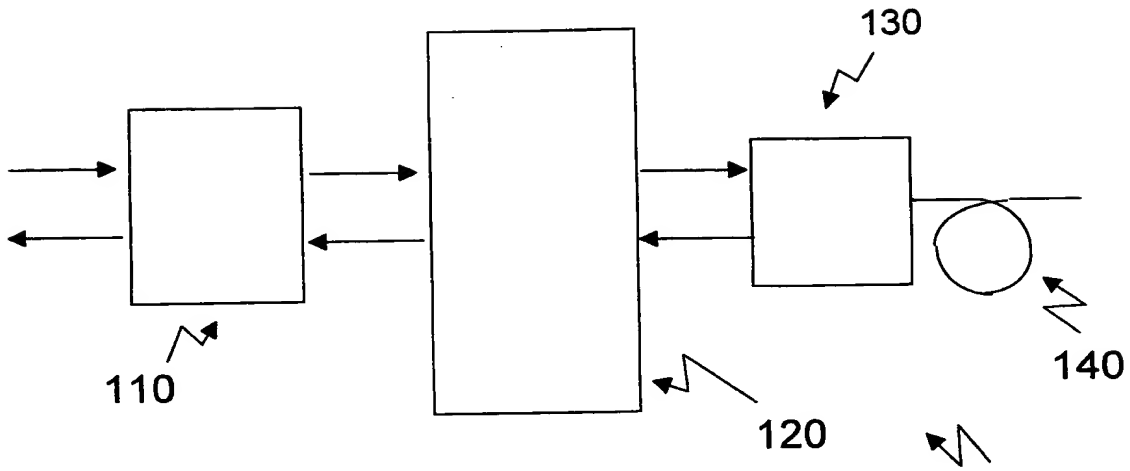

Fig. 1_a

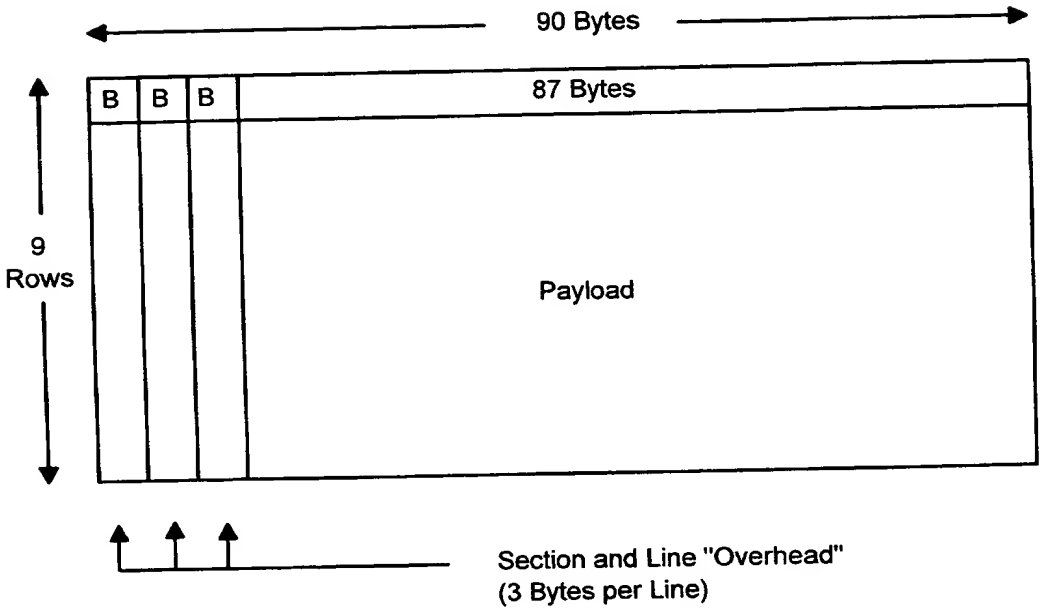
90 Bytes
B
B
B
87 Bytes
9
Rows
Payload
Section and Line "Overhead"
(3 Bytes per Line)

Fig. 1-b.

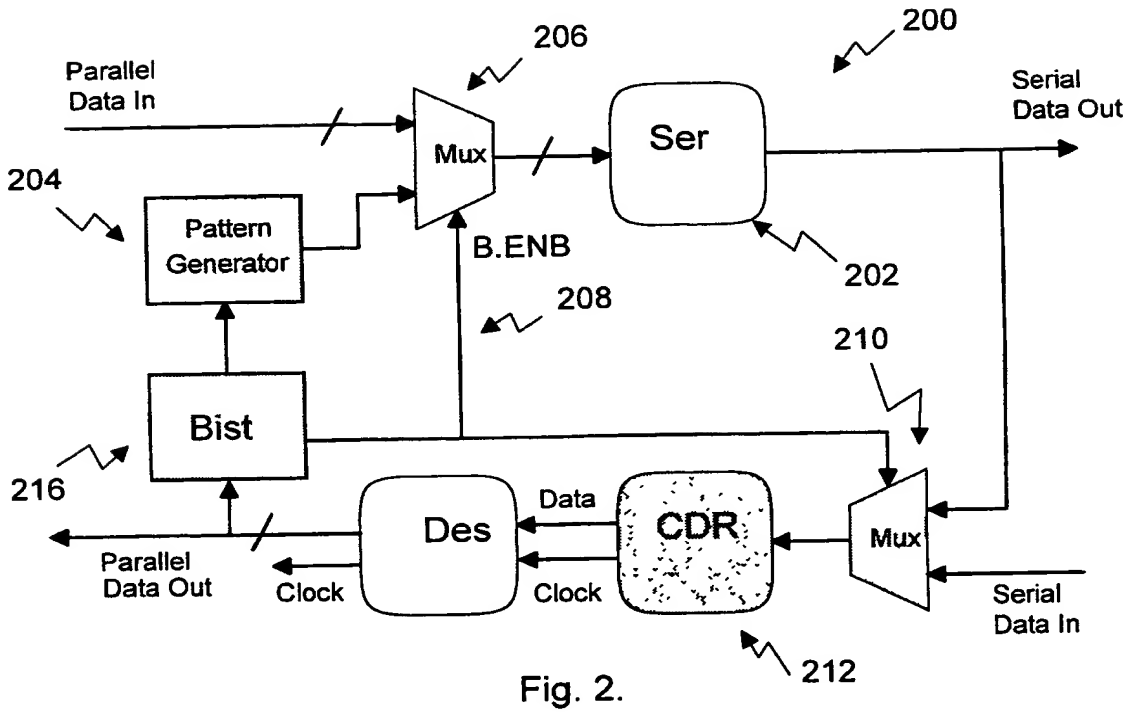
200
206
Parallel
Data In
Mux
Ser
Serial
Data Out
204
Pattern
Generator
B.ENB
202
208
210
Bist
216
Des
Data
CDR
Mux
Parallel
Data Out
Clock
Clock
Serial
Data In
212

Fig. 2.

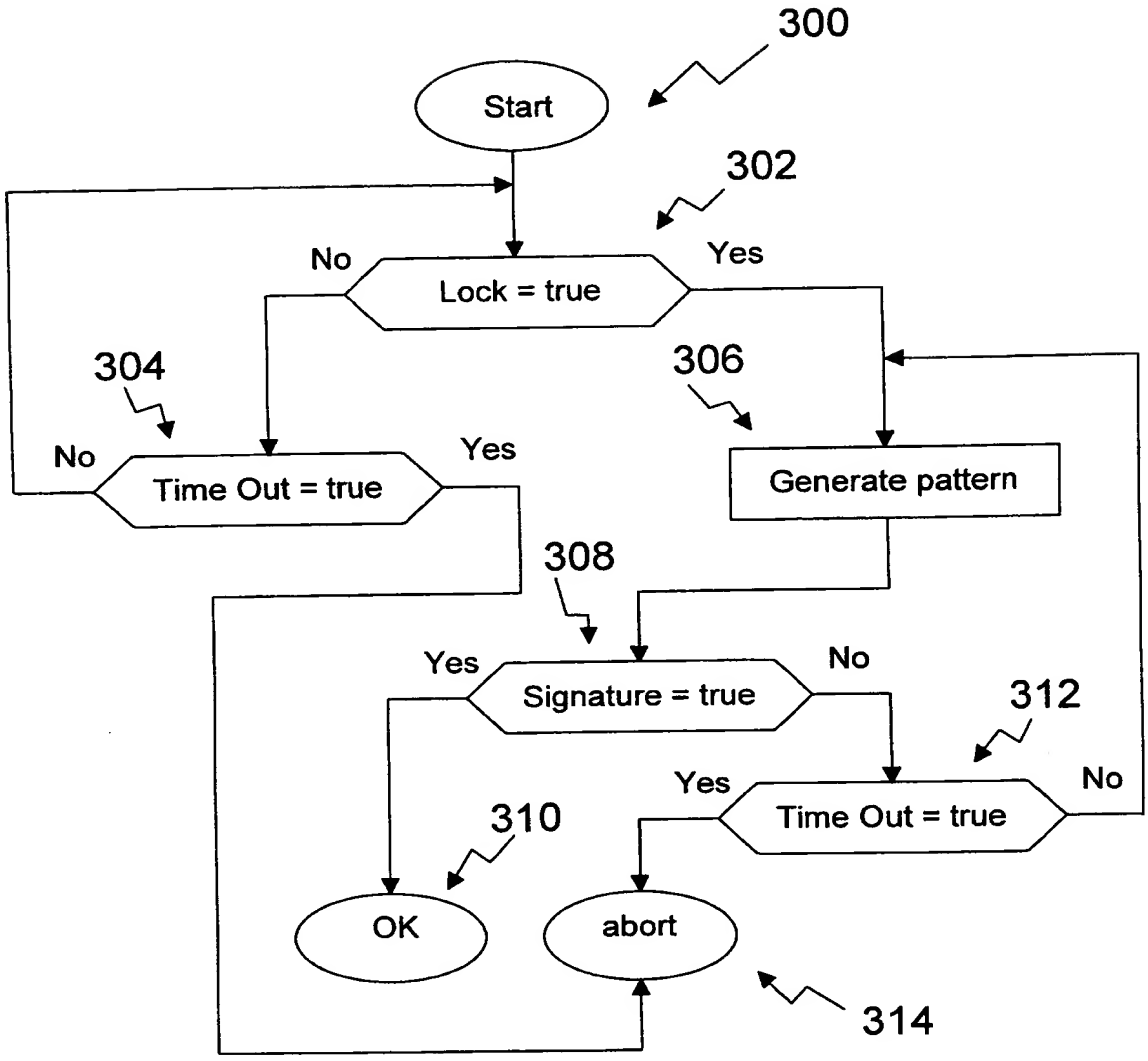
300
Start
302
No
Lock = true
Yes
304
306
No
Time Out = true
Yes
Generate pattern
308
Yes
Signature = true
No
312
Yes
Time Out = true
No
310
OK
abort
314

Fig. 3.